

## CLAIMS

What is claimed is:

1 1. An apparatus, comprising:  
2 two or more parallel carry chain structures within an integrated circuit, each of  
3 said carry chain structures comprising a series of logical structures, at least one  
4 of said logical structures within each of said carry chain structures having an  
5 associated input node, output node and carry node, said input node  
6 corresponding to a function input term, said output node corresponding to an  
7 output term of said function; said carry node corresponding to a carry term to a  
8 following logical structure in said series of logical structures.

1 2. The apparatus of claim 1 wherein said associated input node for one of  
2 said carry chain structures is connected to said associated input node for  
3 another of said carry chain structures.

1 3. The apparatus of claim 1 wherein said logical structure comprises a look  
2 up table.

1 4. The apparatus of claim 3 wherein said look up table is a three input look  
2 up table.

1 5. The apparatus of claim 1 wherein a first functional unit within a first  
2 logical structure performs the same logical operation as a second functional unit  
3 within a second logical structure, said first logical structure within a first carry

4 chain that is parallel to a second carry chain, said second carry chain having  
5 said second logical structure.

1 6. The apparatus of claim 3 wherein said logical structure comprises two  
2 look up tables.

1 7. The apparatus of claim 6 wherein said carry node is coupled to one of  
2 said look up tables and said output node is coupled to the other of said look up  
3 tables.

1 8. The apparatus of claim 1 wherein said function is an incrementer.

1 9. The apparatus of claim 1 wherein said function is an adder.

1 10. The apparatus of claim 1 wherein said logical structure comprises logic  
2 associated with a standard cell.

1 11. A computer readable medium having stored thereon a data structure  
2 associated with a semiconductor design tool, comprising:  
3 two or more parallel carry chain structures, each of said carry chain  
4 structures comprising a series of logical structures, at least one of said logical  
5 structures within each of said carry chain structures having an associated input  
6 node, output node and carry node, said input node corresponding to a function  
7 input term, said output node corresponding to an output term of said function;  
8 said carry node corresponding to a carry value to a following logical structure  
9 in said series of logical structures.

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1 12. The machine readable medium of claim 11 wherein said associated input  
2 node for one of said carry chain structures is connected to said associated input  
3 node for another of said carry chain structures.

1 13. The machine readable medium of claim 11 wherein said logical structure  
2 comprises a look up table associated with programmable logic technology.

1 14. The machine readable medium of claim 13 wherein said look up table is  
2 a three input look up table.

1 15. The machine readable medium of claim 13 wherein a first functional unit  
2 within a first logical structure performs the same logical operation as a second  
3 functional unit within a second logical structure, said first logical structure  
4 within a first carry chain that is parallel to a second carry chain, said second  
5 carry chain having said second logical structure.

1 16. The machine readable medium of claim 13 wherein said logical structure  
2 comprises two look up tables.

1 17. The machine readable medium of claim 16 wherein said carry node is  
2 coupled to one of said look up tables and said output node is coupled to the  
3 other of said look up tables.

1 18. The machine readable medium of claim 11 wherein said function is an  
2 incrementer.

1 19. The machine readable medium of claim 11 wherein said function is an  
2 adder.

1 20. The machine readable medium of claim 11 wherein said logical structure  
2 comprises logic associated with a standard cell.

1 21. A method, comprising:

2 a) presenting input terms of a function to a two or more parallel  
3 carry chain structures;  
4 b) executing each of said two or more parallel carry chain structures  
5 in parallel;  
6 c) collecting the output terms of said function from said two or more  
7 parallel carry chain structures.

1 22. The method of claim 21 wherein all of said input terms are presented to  
2 each of said two or more parallel carry chain structures.

1 23. The method of claim 21 wherein a carry term produced by a logical  
2 structure associated with one of said carry chain structures is ANDed, within  
3 another logical structure associated with said one of said carry chain structures,  
4 with one of said input terms.

1 24. The method of claim 23 wherein said AND produces another carry term.

1 25. The method of claim 21 wherein said function is an incrementer.

1 26. A method, comprising:

2 a) searching for a carry chain within a semiconductor device design;

3 b) determining a first propagation delay through a found carry chain

4 found, said found carry chain found from said searching;

5 c) determining a second propagation delay through a parallel carry

6 chain implementation of said found carry chain; and

7 d) replacing said found carry chain within said semiconductor

8 device design with said parallel carry chain implementation if said second

9 propagation delay is lower than said first propagation delay.

1 27. The method of claim 26 wherein said semiconductor device design is an

2 RTL netlist.

1 28. The method of claim 29 wherein said pre-determined amount is 50% of

2 said first propagation delay.

1 29. The method of claim 26 further comprising searching for a second carry

2 chain within said semiconductor device design after said replacing.

1 30. The method of claim 26 wherein said found carry chain and said parallel

2 carry implementation perform the function of an incrementer.

1 31. The method of claim 26 wherein said found carry chain and said parallel

2 carry implementation perform a decoding function for a multiplexer within a

3 multiplier.

1 32. A method comprising:  
2 within a semiconductor device design environment, responding to a  
3 selection of a function by implementing at least a portion of said function as one  
4 or more parallel carry chains.

1 33. The method of claim 32 wherein said at least a portion of said function  
2 determines channel select values for a multiplexer within a multiplier.

1 34. A machine readable medium having stored thereon sequences of  
2 instructions which are executable by a digital processing system, and which,  
3 when executed by the digital processing system, cause the system to perform a  
4 method comprising:

5 a) searching for a carry chain within a semiconductor device design;  
6 b) determining a first propagation delay through a found carry chain  
7 found, said found carry chain found from said searching;  
8 c) determining a second propagation delay through a parallel carry  
9 chain implementation of said found carry chain; and  
10 d) replacing said parallel carry chain implementation within said  
11 semiconductor device if said second propagation delay is lower than said first  
12 propagation delay.

1 35. The machine readable medium of claim 34 wherein said semiconductor  
2 device design is an RTL netlist.

1 36. The machine readable medium of claim 35 further comprising compiling  
2 a behavioral level netlist to produce said RTL netlist.

1 37. The machine readable medium of claim 34 further comprising searching  
2 for a second carry chain within said semiconductor device design after said  
3 replacing.

1 38. The machine readable medium of claim 34 wherein said found carry  
2 chain and said parallel carry implementation perform the function of an  
3 incrementer.

1 39. The machine readable medium of claim 34 wherein said found carry  
2 chain and said parallel carry implementation perform a decoding function for a  
3 mutliplexer within a multiplier.

1 40. A machine readable medium having stored thereon sequences of  
2 instructions which are executable by a digital processing system, and which,  
3 when executed by said digital processing system, cause said system to perform  
4 a method, comprising:

5 within a semiconductor device design environment, responding to a  
6 selection of a function by implementing at least a portion of said function as one  
7 or more parallel carry chains.

1 41. The method of claim 40 wherein said at least a portion of said function  
2 determines channel select values for a multiplexer within a multiplier.

1 42. An apparatus, comprising:  
2 a multiplexer that produces partial products within a multiplier that  
3 multiplies a first word and a second word, said multiplier having a first channel  
4 select input coupled to a first carry chain output and a second channel select  
5 input coupled to a second carry chain output.

1 43. The apparatus of claim 42 wherein said multiplexer further comprises a  
2 selectable channel input of 0.

1 44. The apparatus of claim 42 wherein said multiplexer further comprises a  
2 selectable channel input that corresponds to said word being non shifted.

1 45. The apparatus of claim 44 wherein said first and second carry chains  
2 have input terms corresponding to coefficients of said second word.

1 46. The apparatus of claim 43 wherein said multiplexer further comprises a  
2 selectable channel input that corresponds to said word being shifted.

1 47. The apparatus of claim 46 wherein said first and second carry chains  
2 have input terms corresponding to coefficients of said second word.

1 48. The apparatus of claim 42 wherein said multiplexer further comprises a  
2 selectable channel input that corresponds to a logical inverse of said first word.

1 49. The apparatus of claim 48 wherein said first and second carry chains  
2 have input terms corresponding to coefficients of said second word.

1 50. A machine readable medium having stored thereon sequences of  
2 instructions which are executable by a digital processing system, and which,  
3 when executed by the digital processing system, cause the system to perform a  
4 method comprising:

5 a multiplexer that produces partial products within a multiplier that  
6 multiplies a first word and a second word, said multiplier having a first channel  
7 select input coupled to a first carry chain output and a second channel select  
8 input coupled to a second carry chain output.

1 51. The machine readable medium of claim 50 wherein said multiplexer  
2 further comprises a selectable channel input of 0.

1 52. The machine readable medium of claim 51 wherein said multiplexer  
2 further comprises a selectable channel input that corresponds to said word  
3 being non shifted.

1 53. The machine readable medium of claim 52 wherein said first and second  
2 carry chains have input terms corresponding to coefficients of said second  
3 word.

1 54. The machine readable medium of claim 51 wherein said multiplexer  
2 further comprises a selectable channel input that corresponds to said word  
3 being shifted.

1 55. The machine readable medium of claim 54 wherein said first and second  
2 carry chains have input terms corresponding to coefficients of said second  
3 word.

1 56. The machine readable medium of claim 42 wherein said multiplexer  
2 further comprises a selectable channel input that corresponds to a logical  
3 inverse of said first word.

1 57. The apparatus of claim 48 wherein said first and second carry chains  
2 have input terms corresponding to coefficients of said second word.